**LAB lists for CA BSc CSIT 3rd Sem**

LAB1. Verify the 1's and 2's complement operations of computer system by using c or c++ codes.

LAB2. Verify the Multiplication of Signed Magnitude data of computer system by using c or c++ codes.

LAB3. Verify Booth multiplication algorithm of computer system by using c or c++ codes.

LAB4. Verify Restoring Division Algorithm of computer system by using c or c++ codes.

LAB5. Verify Non-Restoring Algorithm of computer system by using c or c++ codes.

LAB6. Design the schematic diagram of Logic gates (AND, OR, NOT gate) and verify its relevant truth table using Xilinx software. Write the necessary VHDL codes for Schematic and timing diagram (test bench).

LAB7. Design the schematic diagram of Half Adder and Full Adder .Also, verify its relevant truth table using Xilinx software. Write the necessary VHDL codes for Schematic and timing diagram (test bench).

LAB8. Design the schematic diagram of Encoder and Decoder. Also, verify its relevant truth table using Xilinx software. Write the necessary VHDL codes for Schematic and timing diagram (test bench).

LAB9. Design the schematic diagram of 4x1 MUX and 1x4 DMUX .Also, verify its relevant truth table using Xilinx software. Write the necessary VHDL codes for Schematic and timing diagram (test bench).

LAB10. Design the schematic diagram of 4-bit ALU that verifies the logical operations: AND, NAND and OR. Also, verify its relevant truth table using Xilinx software. Write the necessary VHDL codes for Schematic and timing diagram (test bench).